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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,765	12/03/2003	S. Brad Herner	MA-070-1	7587

7590 08/22/2006

Matrix Semiconductor, Inc.
3230 Scott Blvd
Santa Clara, CA 95054

EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,765	HERNER, S. BRAD	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-20,27,28,30-44 and 57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-20, 27, 28, 30-44 and 57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/08/06 has been entered.

Claim Objections

Claim 6 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Here, claim 6 does not further limit claim 57. Also, the claim is objected to because it is redundant unto itself by saying that the conductive layer or semiconductor layer is a conductive layer. That is the nature of conductive and semiconductor layers.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 33 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In re claims 33 and 34, the limitations, "for any portion ..." are vague and indefinite because such phrase does not delineate to which portion applicant is referring.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 57, 6 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen (US 2003/0062594 A1).

In re claims 57 and 6, Chen discloses a semiconductor device, comprising:

a silicide layer (56; section [0026]);

a grown dielectric antifuse layer (60, section [0027]) on and in contact with the silicide layer;

a conductive layer (66) on and in contact with the grown dielectric antifuse layer;

wherein the silicide layer and the grown dielectric antifuse layer are portions of the semiconductor device, and wherein the grown dielectric antifuse layer has suffered dielectric breakdown[1], such that an electrical connection exists between the silicide layer and the conductive layer (66).

In re claim 15, Chen discloses the device of claim 6, wherein the conductive layer comprises a metal.

In re claim 16, Chen discloses the device of claim 15, wherein the conductive layer forms a portion of a Schottky diode.

In re claim 17, Chen discloses the device of claim 16 wherein the lightly doped or intrinsic semiconductor layer forms a portion of a Schottky diode after breakdown of the grown dielectric antifuse layer (as in Fig. 11).

In re claim 18, Chen discloses the device of claim 17, wherein the Schottky diode is a portion of a memory cell.

In re claim 19, Chen discloses the device of claim 18, wherein the memory cell is a portion of a memory array.

In re claim 20, Chen discloses the device of claim 19, wherein the memory array is a monolithic three dimensional memory array.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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[1] The inherent purpose of an anti-fuse device.

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 7-14, 27, 28, 30-32, and 35-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (as above).

In re claim 2, Chen discloses the device of claim 57, but does not expressly disclose the type of silicide used. However, the claimed refractory silicide materials are well known in the art and it would have been obvious for one skilled in the art at the time of the invention to choose from any one of well known silicide layers for the purpose, for example, of enhancing the conductivity of a device.

In re claim 3, Chen discloses the device of claim 2, wherein the grown dielectric antifuse layer (ONO) comprises silicon oxide (section [0027]).

In re claim 4, Chen discloses the device of claim 2, wherein the grown dielectric antifuse layer (ONO) comprises nitrogen.

In re claim 5, Chen discloses the device of claim 4, wherein the grown dielectric antifuse layer comprises silicon nitride or silicon oxynitride.

In re claim 7, Chen discloses the device of claim 6, wherein the grown dielectric antifuse layer (60) is less than about 50 angstroms thick (section [0027]).

In re claim 8, Chen discloses the device of claim 6, wherein the silicide rests atop an SOI substrate structure (54). However, it would have been obvious one to one skilled in the art at the time of the invention to use a non-SOI substrate for the purpose, for example, of not isolating the antifuse structure from the lower substrate regions.

In re claim 9, Chen discloses the device of claim 2, but does not expressly disclose the conductor layer being a semiconductor layer. However, semiconductor layers are well known in the art to be used as conductor layers and it would have been obvious for one skilled in the art at the time of the invention to use a semiconductor layer as the top conductor, for the purpose, for example, of less process steps in switching from semiconductor to metal fabrication.

In re claim 10, Chen discloses the device of claim 9, wherein the conductive layer forms a portion of a Schottky diode.

In re claim 11, Chen discloses the device of claim 10 wherein the lightly doped or intrinsic semiconductor layer forms a portion of a Schottky diode after breakdown of the grown dielectric antifuse layer (as in Fig. 11).

In re claim 12, Chen discloses the device of claim 11, wherein the Schottky diode is a portion of a memory cell.

In re claim 13, Chen discloses the device of claim 12, wherein the memory cell is a portion of a memory array.

In re claim 14, Chen discloses the device of claim 13, wherein the memory array is a monolithic three dimensional memory array.

In re claim 27, Chen discloses the device of claim 6, wherein the conductive layer (66) comprises Ti or TiW, but does not expressly disclose the layer comprising TiN. However, it would have been obvious for one of ordinary skill in this art at the time of the invention to use a TiN layer in place of the disclosed layers of Chen for the purpose, for

example, of increasing the resistance of the layer thus making the device easier to control through regulation of voltages.

In re claim 28, Chen discloses the device of claim 27, wherein the conductive layer forms a portion of a Schottky diode.

In re claim 30, Chen discloses the device of claim 28, wherein the Schottky diode is a portion of a memory cell.

In re claim 31, Chen discloses the device of claim 30, wherein the memory cell is a portion of a memory array.

In re claim 32, Chen discloses the device of claim 31, wherein the memory array is a monolithic three dimensional memory array.

In re claim 35, Chen discloses the device of claim 2, wherein the grown dielectric antifuse layer was grown by oxidizing the silicide (section [0027]).

In re claim 36, Chen discloses the device of claim 2, wherein the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between a Schottky diode and a conductor.

In re claim 37, Chen discloses the device of claim 36, wherein the conductive layer forms a portion of a Schottky diode.

In re claim 38, Chen discloses the device of claim 37, wherein the Schottky diode is a portion of a memory cell.

In re claim 39, Chen discloses the device of claim 38, wherein the memory cell is a portion of a memory array.

In re claim 40, Chen discloses the device of claim 36, wherein the silicide is a portion of the Schottky diode.

In re claim 41, Chen discloses the device of claim 2, wherein the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

In re claim 42, Chen discloses the device of claim 41, wherein the Schottky diode is a portion of a memory cell.

In re claim 43, Chen discloses the device of claim 42, wherein the memory cell is a portion of a memory array.

In re claim 44, Chen discloses the device of claim 43, wherein the memory array is a monolithic three dimensional memory array.

Response to Arguments

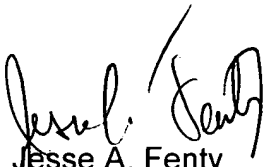
Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on M-F 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Jesse A. Fenty
AU 2815